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# IMPLEMENTATION ASPECTS OF A SEQUENTIAL AC/DC POWER FLOW COMPUTATION ALGORITHM FOR MULTI-TERMINAL VSC HVDC SYSTEMS

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## Abstract

In this paper, the implementation of a sequential AC/DC power flow computation algorithm for Multi-terminal Voltage Source Converter High Voltage Direct Current (VSC MTDC) systems is discussed. The already available models for two-terminal Voltage Source Converter High Voltage Direct Current (VSC HVDC) presented in literature have certain shortcomings and are often not general enough, which can impede their extension to MTDC models. Due to a general formulation of the problem, the proposed algorithm allows to incorporate multiple DC grids with arbitrary topologies. The algorithm includes converter station losses and allows to access the DC grid variables in a way similar to AC power flow programs.

## 1 Introduction

The power engineering world is showing an increasing interest in transmission schemes based on High Voltage Direct Current (HVDC) technology in Multi-Terminal (MTDC) configurations. Suggestions have been made to construct whole new overlaying DC supergrids to connect the growing share of renewable energy sources. The DC grids could be even offshore, connecting various offshore wind farms and other renewable energy sources. A lot of research has already been carried out on the incorporation of MTDC technology based on Current Source Converter (CSC HVDC) in power flow algorithms [1,2]. Voltage Source Converter High Voltage Direct Current technology (VSC HVDC) has much better prospects for an operation in a multi-terminal configuration than CSC HVDC, hence justifying the need for a general approach. However, the two-terminal VSC HVDC models used in commercial software and presented in literature have certain shortcomings and are often not general enough, which can impede their extension to MTDC models. This paper discusses the implementation of a general sequential AC/DC power flow computation algorithm that can incorporate multiple DC grids with arbitrary grid topologies in AC power flow programs.

The remainder of this paper is organised as follows: In a second section, the assumptions made and the errors introduced in the available approximate models for two-terminal VSC HVDC

systems are illustrated. The paper also discusses the possibilities of extending these approximate models to MTDC systems and summarises earlier attempts to incorporate VSC MTDC models in AC power flows. The third section discusses a fully flexible sequential AC/DC power flow computation algorithm that overcomes the shortcomings of the already available models and is capable of solving multiple MTDC systems. The algorithm elaborates further on the general approach presented in [3], with a focus on the implementation aspects. It is shown that a well thought-out renumbering of both AC and DC buses allows a simple integration of multiple DC grids, which can have fully arbitrary grid topologies with respect to the underlying AC system. The extended algorithm allows to include DC buses without an AC grid connection, as well as converter and line outages. Finally, simulation results are discussed in the fourth section. The results are obtained by integrating the proposed sequential approach into MATPOWER [4], the open source Matlab toolbox.

## 2 VSC HVDC Representation

This section addresses the modelling of both two-terminal VSC HVDC systems and MTDC systems available in literature and commercial software. A first part introduces a general model for a VSC HVDC system. The second part addresses the simplifications that have been made in previously published work and commercial software tools.

### 2.1 System layout

Fig. 1 shows a general 3-phase representation of a VSC Converter station, constituting of a transformer, low pass filters and phase reactors. The filtering requirements are dependent on the technology and on the switching method used to synthesise the converter voltage  $\underline{U}_c$ . Their effect at the fundamental grid frequency can be represented by a shunt capacitor. The recently developed multimodular converter (MMC) approach does not need low pass filtering since the voltage waveforms can be synthesised without a Pulse Width Modulation (PWM) technique. In this paper, the filters are not included. They can be easily represented by shunt capacitances at the filter bus, as done in commercial software tools such as PSS/E.

The converter equations reduce to these of an impedance with a controllable converter voltage. With  $\underline{U}_s = U_s \angle \delta_s$  the AC

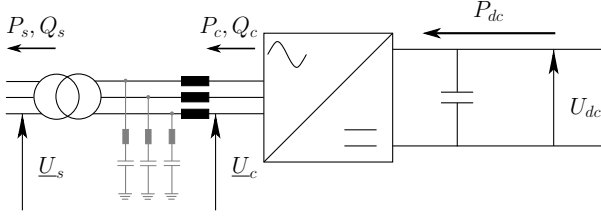


Figure 1. General VSC HVDC converter station.

bus voltage,  $\underline{U}_c = U_c \angle \delta_c$  the converter bus voltage and  $\underline{Z}_c = G_c + jB_c$  the complex equivalent impedance, the equations for the power injected into the AC grid are given by

$$P_s = -U_s^2 G_c + U_s U_c [G_c \cos(\delta_s - \delta_c) + B_c \sin(\delta_s - \delta_c)], \quad (1)$$

$$Q_s = -U_s^2 B_c + U_s U_c [G_c \sin(\delta_s - \delta_c) - B_c \cos(\delta_s - \delta_c)]. \quad (2)$$

The power flowing to the AC network at the converter end can be written as

$$P_c = U_c^2 G_c - U_s U_c [G_c \cos(\delta_s - \delta_c) - B_c \sin(\delta_s - \delta_c)], \quad (3)$$

$$Q_c = -U_c^2 B_c + U_s U_c [G_c \sin(\delta_s - \delta_c) + B_c \cos(\delta_s - \delta_c)]. \quad (4)$$

A general converter model should also incorporate the converter losses, which are taken into account in this paper by a formula quadratically depending on the converter current  $I_c$  [5]. As shown in the remainder of this paper, the inclusion of the converter losses introduces an additional iterative calculation in the sequential AC/DC power flow.

With regard to the AC grid, the converter can either control its reactive power output ( $Q$ -control) or adapt its reactive power output to keep up the voltage at the system bus ( $V$ -control). All converters can also independently control their active power injection ( $P$ -control). In a two-terminal VSC HVDC system, one of the two converters is assigned the task of the DC slack and it therefore adapts its active power output to keep up its DC voltage  $U_{dc}$ . Extending this principle to a MTDC system with  $n$  buses, results in one DC slack bus per DC grid and  $n - 1$  buses that can be either in  $PV$  or  $PQ$ -control.

Contrary to stability studies [6], the DC capacitor can be omitted, as well as the distributed DC line capacitance and inductance since only steady state is addressed. All DC lines can thus be represented as lumped resistances if leakage currents are neglected.

## 2.2 Simplified steady-state models

A two-terminal VSC HVDC link can be incorporated in power flow programs in different ways. The complexity of the combined AC/DC power flow algorithm depends on the details of the model and on the assumptions. This part briefly discusses different representations and addresses how assumptions and simplifications can impede the extension of these models to a MTDC system.

As discussed above, a VSC can be represented in power flow programs as a voltage source behind a reactance. The VSC therefore shows a steady-state behaviour that is similar to that of a synchronous generator. When the power injections are defined with respect to the system bus instead of the converter bus, as is

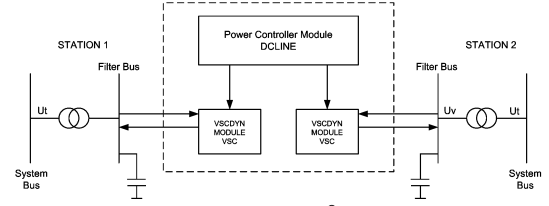


Figure 2. PSS/E model [7].

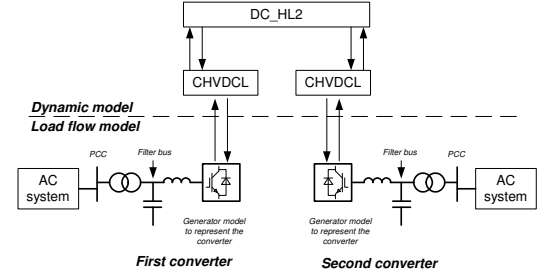


Figure 3. HVDC Light model [8].

often done to simplify calculations, the VSC can be represented as a  $PQ$  node or as a  $PV$  node when under voltage control. However, there exists a relationship between the active powers of the different converters as the slack bus converter adapts its power output to keep up the DC grid voltage. For a two-terminal system, the slack bus active power setpoint  $P_{s,1}^*$  can be written as  $P_{s,1}^* = P_{s,1} - P_{loss}$  with  $P_{loss}$  the overall system losses, including both converter losses and DC line losses. This simplified two-terminal model is often used in commercial software due to its easy integration in existing power flow algorithms. As a disadvantage, the DC system is not accessible and all information on internal DC variables is therefore lacking. As the overall VSC HVDC system losses are not known beforehand, the overall results are only as good as the approximation of these losses.

Two commercially available VSC HVDC models, both implemented in PSS/E, are briefly discussed in the remainder of this part to make a comparison with the generalised model discussed in this paper. The first model comes with PSS/E. The second model, the ABB HVDC Light model [8], is a manufacturer developed model. The PSS/E model in Fig. 2 consists of three modules: two converter modules and a DC line model. The power injections and voltage setpoint are specified with respect to the filter bus. Transformers and filters have to be modelled explicitly by adding a transformer branch and a fixed or switched shunt reactance at the filter bus. The model does not support multi-terminal calculations. The PSS/E model is of the simplified type, with a few additions such as operating limits and a loss model. The HVDC Light model, represented in Fig. 3, has been developed to serve as a starting point for dynamic simulations. The converters are modelled as generators and no DC line is modelled. The model is thus of the simplified type. As in the PSS/E model, filters and transformers are added separately. In both models, the converter bus is not accessible. The PSS/E model includes a linear loss model, whereas the HVDC Light model does not include losses.

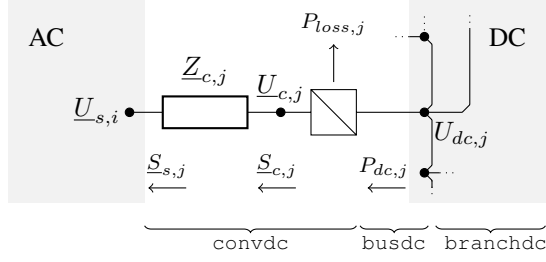


Figure 4. Subdivision of the DC system data in matrices.

Due to the simplifications in available models, there is a need for a more general approach to include DC grids in power flow calculations. Most of the methods previously presented in literature are not general enough and suffer from the same drawbacks as the commercial models: In [9] an approximate solution is obtained by neglecting converter losses and losses in the phase reactor, whereas in [10] converter losses are neglected, DC variables are not accessible and the power flow setpoints are defined at the converter bus instead of the system bus. This simplifies the calculations, but is not in accordance with current practice in actual VSC HVDC systems. A unified power flow approach was presented in [11]. However, the DC grid was not explicitly represented in the model. The next sections discuss the implementation aspects and mathematical modelling of a more general representation of VSC MTDC grids.

### 3 VSC MTDC Implementation

In this part, the implementation of a general AC/DC power flow algorithm [3] is discussed. Meanwhile, the algorithm is extended and a bus renumbering algorithm is proposed to introduce floating DC buses without a connection to the underlying AC grid. The extension also allows an easy integration of multiple DC grids, converter outages and branch outages. After presenting the data input together with the bus renumbering, a second part of this section addresses the modelling of the DC grid, the interconnection with the AC grid and the sequential power flow procedure.

#### 3.1 Data input and preparation

The DC network data and converter parameters are handled in a way similar to the AC network representation in MATPOWER, where a distinction is made between `bus`, `gen` and `branch` matrices. They respectively contain all data of the AC buses, the synchronous generators and the AC lines and cables. The AC/DC power flow program adds `busdc`, `convdc` and `branchdc` matrices to this set, which fulfill a similar role in the DC grid as their AC counterparts do in the AC grid. Fig. 4 shows how all DC power flow data is related to these matrices for an arbitrary converter linking AC bus  $i$  and DC bus  $j$ . Similar to the `bus` matrix in the AC power flow, the `busdc` matrix contains power injections and bus voltages. The matrix also contains information on the connection of the DC buses with AC buses. The `convdc` matrix contains all converter data and forms the actual link between the AC and DC grids. The matrix contains input data such as loss coefficients and converter

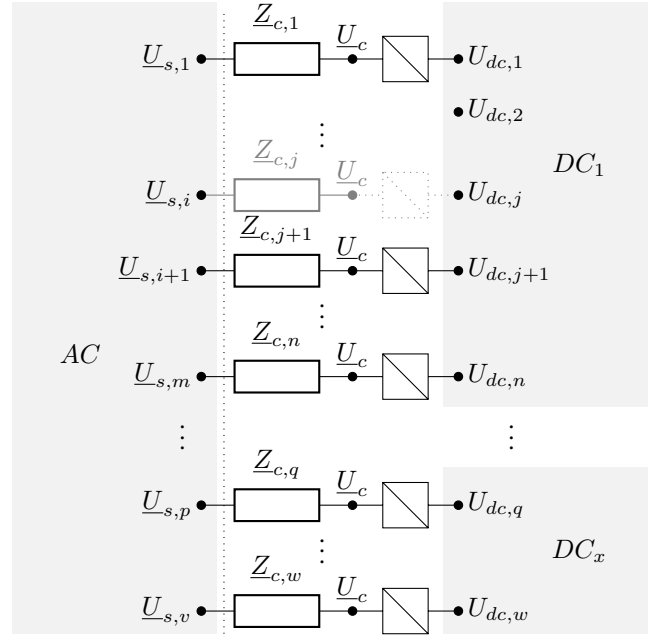


Figure 5. AC-DC interconnection scheme.

reactances as well as output data such as converter losses and powers and voltages at the converter bus. The converters fulfill a role to the DC grid similar to that of the generators in an AC grid. Finally, matrix `branchdc` links the different DC buses and contains all line parameters.

Fig. 5 shows the interconnection of an AC grid with  $v$  buses and  $x$  DC grids with a total of  $w$  buses. Without lack of generality, we assume the last AC bus  $v$  to be connected to the  $x$ -th DC grid. With  $v > w$ , there are  $v - w$  AC buses without a connection to a DC grid. The DC buses have been numbered in a logical order for convenience, although the algorithm does not impose any restrictions to the numbering of the DC buses as such. Each grid can have an arbitrary number of converter-connected DC buses, as well as DC buses without an AC interconnection (e.g. DC bus 2 in grid 1) and DC buses facing a converter outage (e.g. DC bus  $j$  in grid 1). The numbering of all converter data refers to the corresponding DC bus.

The different bus indices for the AC grid and the DC grids result in a maximum flexibility for the user to enter the different grid layouts in the power flow algorithm. However, this double numbering hampers a straight-forward implementation of the algorithm. After a per unit conversion of the AC and DC grid quantities, the sorting algorithm depicted in Fig. 6 renames the DC and AC buses to overcome these difficulties. After renumbering the DC buses and sorting them per DC grid, the algorithm groups converter-connected DC buses and renames their AC buses correspondingly, e.g. buses 1 to  $k$  for the first DC grid in Fig. 6. Thereafter, arbitrary AC buses without DC connections are assigned to the DC buses without an AC connection, e.g. buses  $k + 1$  to  $n$  in Fig. 6. All converter outages are considered equally to DC buses without a converter. The renumbering allows an easy and straightforward access to both AC grid and DC grid variables during the power flow without compromising the flexibility of the user interface. The

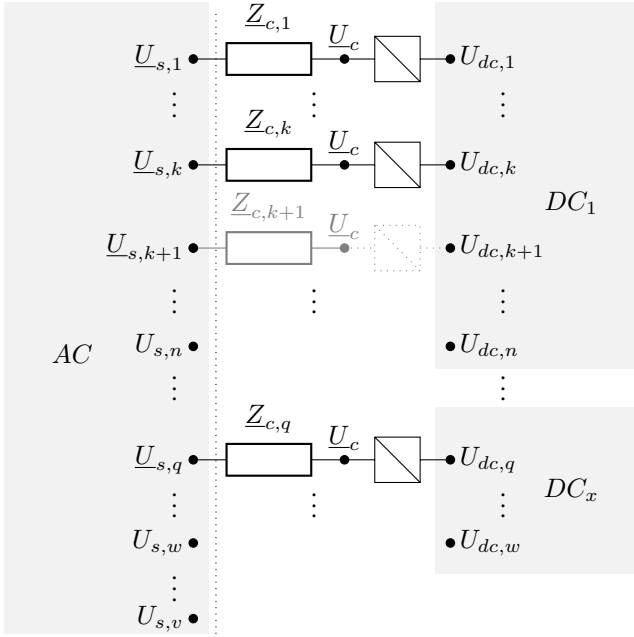


Figure 6. AC-DC interconnection scheme after renumbering.

next section briefly discusses the mathematical modelling of the sequential power flow algorithm.

### 3.2 Mathematical modelling

Fig. 7 shows the flow chart of the sequential power flow algorithm. The converter power injections  $P_s$  and  $Q_s$  are included in the power mismatch vectors  $\Delta P^{(k)}$  and  $\Delta Q^{(k)}$  of the Newton-Raphson power flow algorithm as negative loads:

$$\Delta P_i^{(k)} = P_i^{gen} - (P_i^{dem} - P_{s,i}) - P_i(U^{(k)}, \delta^{(k)}), \quad (5)$$

$$\Delta Q_i^{(k)} = Q_i^{gen} - (Q_i^{dem} - Q_{s,i}) - Q_i(U^{(k)}, \delta^{(k)}). \quad (6)$$

Dummy AC generators are included for converters in  $V$ -control, as their reactive power injection is unknown prior to the AC power flow. Meanwhile, the AC buses to which these converters are connected, are changed from  $PQ$ -nodes into  $PV$ -nodes.

The active power injection  $P_s$  of the DC slack buses is adapted to keep up the voltage of the DC grids. As a first estimate, all converter stations as well as the DC grids are assumed to be lossless. To simplify notation, but without loss of generality, we assume the first converter of every grid to be the DC slack bus converter. Hence, for the first DC grid, we can write:

$$P_{s,1}^{(0)} = - \sum_{j=2}^k P_{s,j}. \quad (7)$$

For the  $k^{th}$  iteration, the solution from the previous iteration cycle is used as an estimate for  $P_{s,1}^{(k)}$ .

After calculating all converter side powers  $\underline{S}_c$ , voltages  $\underline{U}_c$  and converter losses  $P_{loss}$ , the power injections into the DC grids are known.

The power flows in the DC grid itself can be obtained in a way similar to those in an AC grid. The current injected at a DC

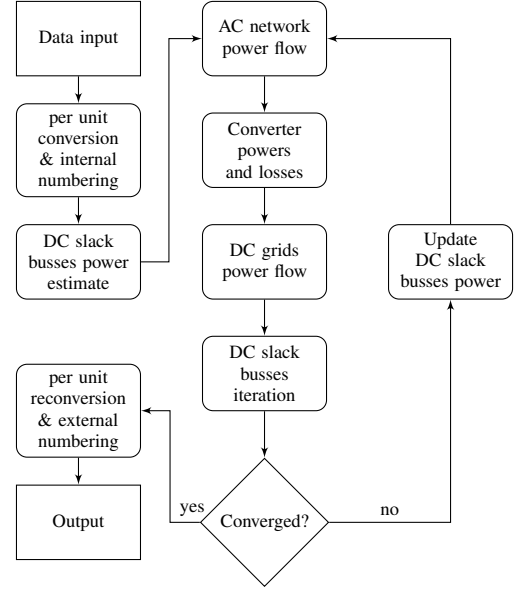


Figure 7. Flow chart of the sequential VSC AC/DC power flow algorithm.

node  $i$  can be written as the current flowing to the other  $n - 1$  nodes in the network:

$$I_{dc,i} = \sum_{\substack{j=1 \\ j \neq i}}^n Y_{dc,ij} \cdot (U_{dc,i} - U_{dc,j}), \quad (8)$$

with  $Y_{dc,ij}$  equal to  $1/R_{dc,ij}$ .

Combining all currents injected in the DC network results in

$$\mathbf{I}_{dc} = \mathbf{Y}_{dc} \mathbf{U}_{dc}, \quad (9)$$

with  $\mathbf{I}_{dc} = [I_{dc,1}, I_{dc,2}, \dots, I_{dc,k}, 0, \dots, 0]^T$  the DC current vector with  $n - k$  zero elements due to floating DC buses and converter outages,  $\mathbf{U}_{dc} = [U_{dc,1}, U_{dc,2}, \dots, U_{dc,n}]^T$  the DC voltage vector and  $\mathbf{Y}_{dc}$  the DC bus matrix. When line outages are taken into account, the DC bus matrix needs to be updated accordingly. Assuming a monopolar, symmetrically grounded DC grid, the active power injected in node  $i$  can be written as

$$P_{dc,i} = 2U_{dc,i} I_{dc,i}, \quad \forall i \leq k. \quad (10)$$

The current injections  $\mathbf{I}_{dc}$  are not known prior to the power flow solution for the DC grid, whereas the active power injections  $\mathbf{P}_{dc}$  are known for all buses except for the DC slack bus as a results of the AC power flow. Combining (9) and (10) results in a system of non-linear equations:

$$0 = \mathbf{Y}_{dc} \mathbf{U}_{dc} - \left[ \frac{P_{dc,i}}{2U_{dc,i}} \right], \text{ with } P_{dc,i} = 0 \quad \forall i > k. \quad (11)$$

With the first converter as the DC slack bus, the vector of the unknowns can now be written as

$$\mathbf{X} = \begin{bmatrix} X_1 \\ \mathbf{X}_2 \end{bmatrix} = \begin{bmatrix} \frac{P_{dc,1}}{U_{dc,2}} \\ \vdots \\ U_{dc,n} \end{bmatrix}. \quad (12)$$

The DC bus admittance matrix of the first DC grid is partitioned

as follows:

$$\mathbf{Y}_{dc} = \begin{bmatrix} y_{11} & \mathbf{Y}_{12} \\ \mathbf{Y}_{21} & \mathbf{Y}_{22} \end{bmatrix}, \quad (13)$$

with  $y_{11}$  a scalar,  $\mathbf{Y}_{12}$  a row vector of length  $n-1$ ,  $\mathbf{Y}_{21}$  a column vector of length  $n-1$ , and  $\mathbf{Y}_{22}$  a matrix of dimension  $(n-1) \times (n-1)$ .

This leads to a system of equations that can be solved by an iterative Newton method:

$$0 = y_{11} \cdot u_{dc,ref} + \mathbf{Y}_{12} \mathbf{X}_2 - X_1 / (2u_{dc,ref}) \quad (14)$$

$$0 = \mathbf{Y}_{21} \cdot u_{dc,ref} + \mathbf{Y}_{22} \mathbf{X}_2 - \mathbf{I}_2, \quad (15)$$

with

$$\mathbf{I}_2 = \left[ \frac{P_{dc,2}}{2X_2}, \frac{P_{dc,3}}{2X_3}, \dots, \frac{P_{dc,k}}{2X_k}, 0, \dots, 0 \right]^T. \quad (16)$$

Explicitly representing the DC circuit without a prior knowledge of the injected currents thus results in an additional iterative calculation.

The same methodology can now be applied to all other DC grids. Combining all DC bus matrices  $\mathbf{Y}_{dc,j}$  of the DC grids in one matrix results in a sparse band matrix  $\mathbf{Y}_{dc}$ :

$$\mathbf{Y}_{dc} = \begin{bmatrix} \mathbf{Y}_{dc1} & & \\ & \ddots & \\ & & \mathbf{Y}_{dcx} \end{bmatrix}. \quad (17)$$

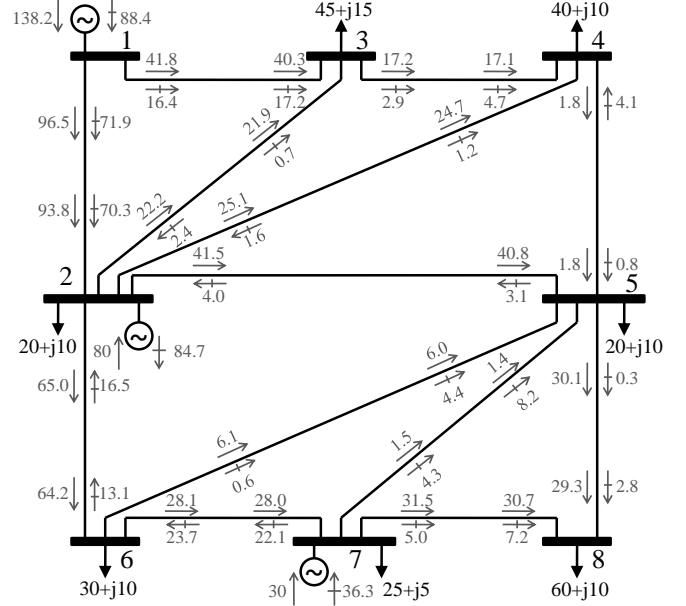
Writing (14) – (15) for all DC grids results in a system of  $w$  equations, with  $x$  equations in the form of (14), that can be jointly solved with one iterative method. After convergence, the DC line currents can easily be obtained by premultiplying the DC bus voltage vector  $\mathbf{U}_{dc}$  by the system branch admittance matrices  $\mathbf{Y}_{dcf}$  and  $\mathbf{Y}_{dct}$ , which are obtained as a byproduct of the construction of the DC bus matrix  $\mathbf{Y}_{dc}$ .

After solving the DC network power flow, an additional iterative calculation is needed to recalculate the slack buses' power injections into the AC grid. In [3], it was suggested not to alter the AC grid state during this additional iteration: the grid side voltage of all slack buses  $\underline{U}_{s,1}$  is thus kept constant (both in magnitude and phase angle), as well as the reactive power grid injection  $Q_{s,1}$ , while the converter active power injection  $P_{c,1}$  is iteratively updated. As an alternative to this approach, the reactive power injection at the converter bus  $Q_{c,1}$  can be kept constant as well. However, it was found that a constant value of  $Q_{s,1}$  results in less overall iteration cycles, due to the stronger relationship between  $Q_{s,1}$  and  $U_{s,1}$ , which is also kept constant during one overall iteration cycle.

After a convergence of all slack buses' power injections, the AC grid values are updated until overall convergence is reached.

## 4 Simulation results

The proposed AC/VSC MTDC power flow algorithm has been integrated with MATPOWER [4], an open source Matlab based AC power flow program. Simulations were carried out with two VSC HVDC systems in an 8-bus test network, based on the 5-bus model presented in [12], as well as with multiple DC grids in the case2746wp bus network [4], which represents



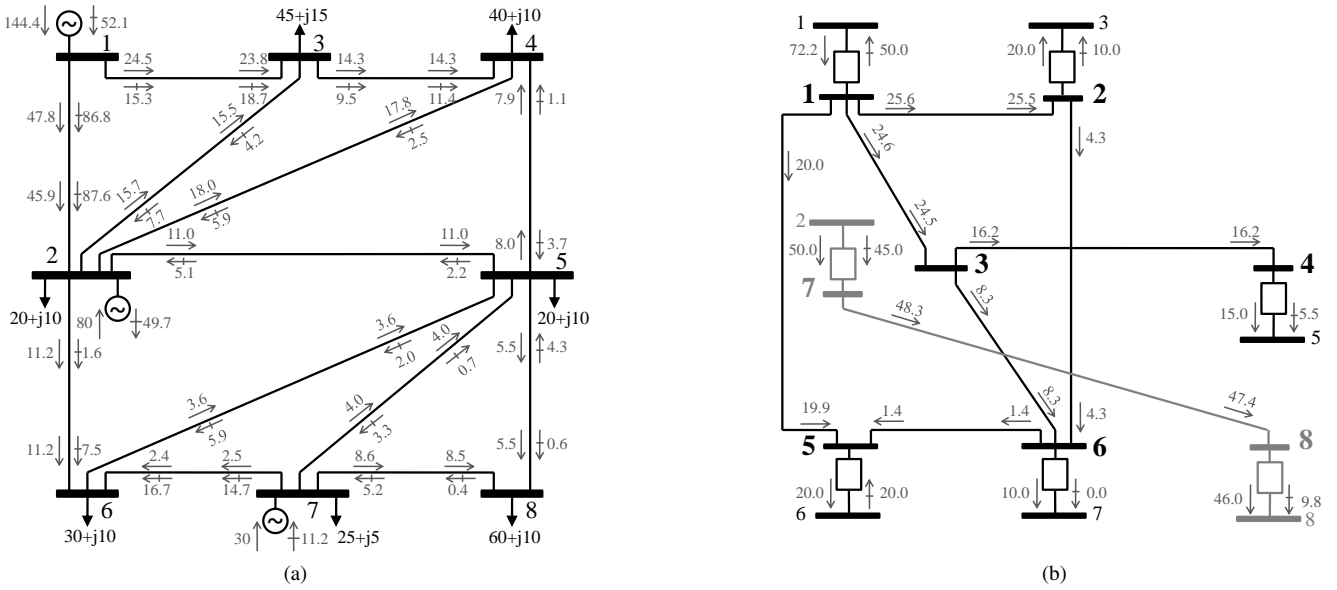


Figure 9. Power flow solution with the VSC MTDC systems : (a) Line powers in the 8-bus test network, (b) Line powers and AC grid injections of the VSC MTDC systems. **Legend:**  $\rightarrow$  Active power (MW) and  $\rightarrow$  Reactive power (MVAR).

DC bus	Control mode	Converter Voltage		Converter powers		Reactor loss		Converter loss	DC Power	DC Voltage
		$U_c$ (p.u.)	$\delta_c$ (deg)	$P_c$ (MW)	$Q_c$ (MVar)	$P$ (MW)	$Q$ (MVar)	$P_{loss}$ (MW)	$P_{dc}$ (MW)	$U_{dc}$ (p.u.)
1	Slack - Q	1.162	-6.76	-72.12	63.72	0.07	13.72	1.85	-70.27	1.000
2	P - Q	1.022	-0.15	20.00	11.00	0.00	1.00	1.20	21.21	0.995
3	-	-	-	-	-	-	-	-	0.00	0.995
4	P - V	1.012	0.28	15.00	6.04	0.00	0.51	1.17	16.17	0.991
5	P - Q	0.956	1.52	20.01	-18.38	0.01	1.62	1.24	21.25	0.993
6	P - Q	1.000	0.19	10.00	0.20	0.00	0.20	1.14	11.14	0.993
7	P - Q	0.915	-6.82	-49.95	-35.95	0.05	9.05	1.64	-48.32	1.020
8	Slack - V	1.024	2.89	46.02	14.24	0.02	4.42	1.36	47.39	1.000

Table 2. Power flow solution with the VSC MTDC systems – Converter stations.

## 5 Conclusion

The general sequential AC/DC power flow algorithm proposed in this paper includes VSC MTDC systems with arbitrary grid topologies in AC power flow programs. Due to a general formulation of the problem and a bus renumbering algorithm, the implementation of the algorithm can also include DC buses without AC connection, as well as converter outages and line outages. The algorithm has been implemented in Matlab and properly tested.

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